

WHAT IS CLAIMED IS:

- 1 1. An integrated circuit comprising:
 - 2 a substrate; and
 - 3 a high electron mobility transistor formed on the substrate, the high
 - 4 electron mobility transistor including a source electrode, a drain electrode and a
 - 5 gate electrode, the high electron mobility transistor having an increased
 - 6 gate-to-drain etch recess spacing, the increased gate-to-drain etch recess spacing
 - 7 proving a greater protection for the high electron mobility transistor from an
 - 8 electrostatic discharge on the drain electrode.
- 1 2. The integrated circuit of claim 1 wherein the high electron mobility
- 2 transistor includes an enhancement mode pseudomorphic high electron mobility
- 3 transistor.
- 1 3. The integrated circuit of claim 2 wherein the increased gate-to-drain etch
- 2 recess spacing is at least four microns.
- 1 4. The integrated circuit of claim 1 further comprising a second high electron
- 2 mobility transistor formed on the substrate on a signal path between an input node
- 3 and an output node, the second high electron mobility transistor having a second
- 4 gate-to-drain etch recess spacing, the gate-to-drain etch recess spacing of the high
- 5 electron mobility transistor being wider than the second gate-to-drain etch recess
- 6 spacing of the second high electron mobility transistor.
- 1 5. The integrated circuit of claim 4 wherein a width of the gate electrode of
- 2 the high electron mobility transistor is wider than a width of a gate electrode of
- 3 the second high electron mobility transistor.
- 1 6. The integrated circuit of claim 1 further comprising a resistor formed over
- 2 the substrate connected to the drain electrode of the high electron mobility
- 3 transistor, the resistor being made of a semiconductor material.

1 7. The integrated circuit of claim 1 further comprising a reverse biased
2 Schottky diode formed over the substrate connected to the drain electrode of the
3 high electron mobility transistor, the reverse biased Schottky diode being
4 configured to have an increased anode-to-cathode etch recess spacing to provide
5 protection for the reverse biased Schottky diode from a positive electrostatic
6 discharge.

1 8. The integrated circuit of claim 7 wherein the reverse biased Schottky diode
2 is structurally configured to turn on prior to the high electron mobility transistor
3 when a negative electrostatic discharge is applied to the drain electrode of the high
4 electron mobility transistor.

1 9. A method for fabricating an integrated circuit with at least one high
2 electron mobility transistor, the method comprising:

3 proving a substrate; and
4 forming a high electron mobility transistor with a source electrode,
5 a drain electrode and a gate electrode on the substrate, including creating an
6 increased gate-to-drain etch recess spacing, the increased gate-to-drain etch recess
7 spacing proving a greater protection for the high electron mobility transistor from
8 an electrostatic discharge on the drain electrode.

1 10. The method of claim 9 wherein the forming of the high electron mobility
2 transistor includes forming an enhancement mode pseudomorphic high electron
3 mobility transistor on the substrate.

1 11. The method of claim 10 wherein the creating of the increased gate-to-drain
2 etch recess spacing includes creating the increased gate-to-drain etch recess
3 spacing of at least four microns.

1 12. The method of claim 9 further comprising forming a second high electron
2 mobility transistor on the substrate on a signal path between an input node and an
3 output node, the second high electron mobility transistor having a second
4 gate-to-drain etch recess spacing, the gate-to-drain etch recess spacing of the high
5 electron mobility transistor being wider than the second gate-to-drain etch recess
6 spacing of the second high electron mobility transistor.

1 13. The method of claim 12 wherein the forming the high electron mobility
2 transistor includes creating the gate electrode with a width that is wider than a
3 width of a gate electrode of the second high electron mobility transistor.

1 14. The method of claim 9 further comprising forming a resistor over the
2 substrate connected to the drain electrode of the high electron mobility transistor,
3 the resistor being made of a semiconductor material.

1 15. The method of claim 9 further comprising forming a reverse biased
2 Schottky diode over the substrate connected to the drain electrode of the high
3 electron mobility transistor, including creating an increased anode-to-cathode etch
4 recess spacing to provide protection for the reverse biased Schottky diode from a
5 positive electrostatic discharge.

1 16. An integrated circuit comprising:
2 an insulating substrate;
3 a first high electron mobility transistor formed on the insulating
4 substrate, the first high electron mobility transistor having a first gate-to-drain etch
5 recess spacing; and
6 a second high electron mobility transistor formed on the insulating
7 substrate, the second high electron mobility transistor having a second
8 gate-to-drain etch recess spacing that is wider than the first gate-to-drain etch
9 recess spacing of the first high electron mobility transistor to provide a greater
10 protection for the second high electron mobility transistor from an electrostatic
11 discharge.

1 17. The integrated circuit of claim 16 wherein the second gate-to-drain etch
2 recess spacing of the second high electron mobility transistor is at least four
3 microns.

1 18. The integrated circuit of claim 16 wherein a width of a gate electrode of
2 the second high electron mobility transistor is wider than a width of a gate
3 electrode of the first high electron mobility transistor.

1 19. The integrated circuit of claim 16 further comprising a resistor formed
2 over the substrate connected to a drain electrode of the second high electron
3 mobility transistor, the resistor being made of a semiconductor material.

1 20. The integrated circuit of claim 16 further comprising a reverse biased
2 Schottky diode formed over the insulating substrate connected to the second high
3 electron mobility transistor, the reverse biased Schottky diode being configured to
4 have an anode-to-cathode etch recess spacing that is wider than the first
5 gate-to-drain etch recess spacing of the first high electron mobility transistor to
6 provide protection for the reverse biased Schottky diode from the positive
7 electrostatic discharge.